ABSTRACT OF THE DISCLOSURE

A self aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, and an array formed thereby, whereby each memory cell includes a trench formed into a surface of a semiconductor substrate, spaced apart source and drain regions with a channel region formed therebetween. The drain region is formed underneath the trench, and the channel region includes a first portion that extends substantially vertically along a sidewall of the trench and a second portion that extends substantially horizontally along the surface of the substrate. An electrically conductive floating gate is formed over and insulated from at least a portion of the channel region and a portion of the source region. An electrically conductive control gate is formed having a first portion disposed in the trench and a second portion formed over but insulated from the floating gate.